LONG DELAY TRANSISTORIZED TIMER

by Aldo Romano and Piero Alderisio*

FOREWORD

The most satisfactory method of producing a timer having a long delay period is by the use of a Miller integrator circuit followed by a regenerative trigger circuit. The maximum delay obtainable, for a given accuracy, is limited by the low current gain of the transistors used.

By using SGS-Fairchild silicon Planar** transistors, the gain of which remains high even at low collector currents (typical h_{FE} = 200 at I_c = 1 μA), a timer has been produced that is capable of providing variable delays between 1 and 1000 sec with an average error of less than ±2% over a temperature range from 0 to 50°C.

INTRODUCTION

There are three basic methods of producing a transistorized timer of which the most simple arrangement consists in charging a capacitor through a resistor and using the voltage appearing across the capacitor to energize a relay, preferably via a regenerative trigger circuit. Assuming that the threshold voltage V_t of the trigger circuit is subject to an inaccuracy or drift equal to ΔV_t, the voltage must be made as high as possible with respect to ΔV_t in order to reduce the resulting error. Furthermore, the slope of the input voltage rising towards the threshold must be reasonably linear. It is, therefore, obvious that this method requires the aiming V_a, to be much greater than V_t; also, the time constant RC needs to be much greater than the required delay.

A second method uses an RC network followed by an amplifier. In this case V_a can be less than V_t, but the value of RC must still far exceed the required delay. Also, the amplifier must have a high input impedance (≫R), a very stable gain and a negligible thermal drift.

The third, and unquestionably best, method uses a Miller integrator circuit to produce a voltage changing linearly with time. The analysis of this circuit, contained in the Appendix, shows that the time constant can be less than the delay required and the amplifier can have a low input impedance. Furthermore, the stability of the circuit is independent, within wide limits, of the gain of the transistors.

CIRCUIT DESCRIPTION

The circuit diagram of a timer capable of providing delays variable between 1 and 1000s is shown in Fig. 1.

The Miller integrator comprises transistors T_1 and T_2, feedback capacitor C and resistor R, while transistors T_3 and T_4 constitute a trigger circuit capable of operating the relay. With S closed, the circuit is held in the steady state. Because of the voltage drop across R_2 and diode D_1, T_1 is cut off and T_2 is conducting.

The collector current of T_2 is limited by base resistor R_1, whose minimum value is 1MΩ. Because D_2 is reverse-biased, T_3 and T_4 are cut off and the relay is de-energized. The timer is started by opening switch S, which initially causes a tendency for the collector voltage of T_2 to increase rapidly. This change, which is fed back via C to T_1 base, continues until T_1 is brought into conduction. The amplitude ΔV_o of the step voltage is, therefore, approximately equal to the voltage drop across R_2 and D_1 (0.7 ÷ 1V) when the switch was closed, and is given by:

$$\Delta V_o \simeq \frac{R_2}{R_2 + R_3 + R_4} V_{CC} + V_{D1}$$

$$= 0.165 \times 10^{-3} V_{CC} + V_{D1}$$

---

* SGS - Fairchild Applications Laboratory, Agrate, Milan, Italy. As printed in Electronic Components, February 1967.

** Planar is a patented Fairchild process.

COPYRIGHT, FAIRCHILD SEMICONDUCTOR, 1967 • PRINTED IN U.S.A. 3436-009-57 35M

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied.

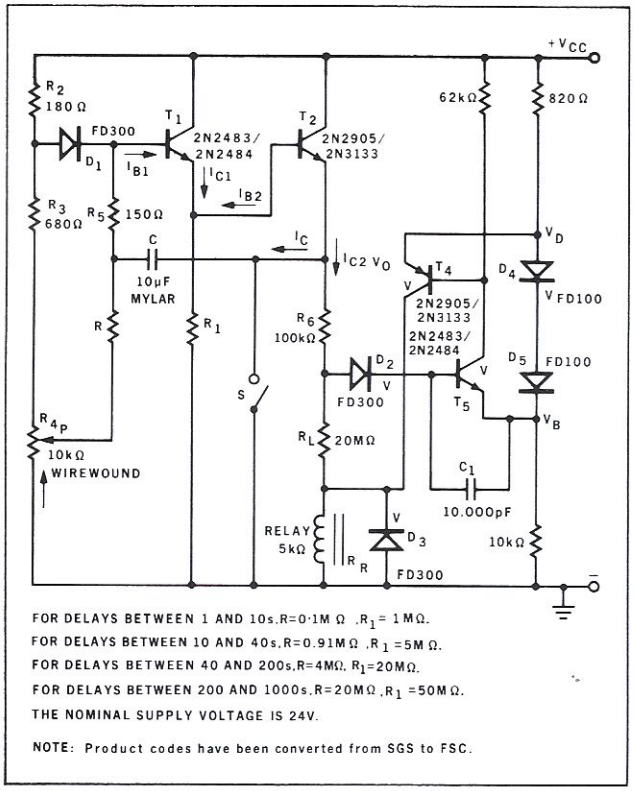

Fig. 1. Long delay transistorized timer.

ignoring both the difference in V_{BE} between T_1 and T_2, and the effect of R_5.

The step voltage present on the base of T_1 places a reverse bias on D_1 and from this instant onwards T_2 collector potential rises linearly until the transistor bottoms (see the Appendix).

When voltage V_A becomes greater than

$$(V_B + V_{BE3} + V_{D2}),$$

T_3 starts to conduct bringing T_4 into conduction. The existence of two positive feedback paths (one to T_3 emitter via D_4 and D_5, the other to T_3 base via the relay and R_L) give rise to a regenerative action that ends with the relay fully energized. Since T_2 collector is a low impedance point, the inclusion of R_6 improves the positive feedback factor.

Diodes D_4 and D_5 perform three functions:

(a) they determine the voltage drop required to switch the trigger circuit without noticeably reducing the positive feedback,

(b) they provide temperature compensation for the trigger circuit,

(c) they cause the threshold level to be almost proportional to the supply voltage.

Capacitor C_1 prevents the trigger from being switched by spurious signals.

Again considering the Miller integrator, it should be noted that the circuit configuration chosen for T_1 and T_2 has the advantage of a low thermal drift. Transistor T_1 operates with a low base-collector voltage that enables its leakage current to be ten times less than the nominal value (measured at 30V). D_1 also operates with a low inverse voltage, with a consequent reduction in the leakage current.

Coarse control of the delay time is effected by switching the resistors R_1 and R, while potentiometer P provides a means of fine control.

The timer is reset by closing switch S. R_5 ensures that the base-emitter junction of T_1 is not reverse biased when this occurs. In order to reduce the collector current I_{c1} of T_1, the value of resistor R_1 should be made very high. Ignoring the values of V_{BE} and the leakage currents, the following equations apply:

$$I_{C2} \cong I_C + \frac{V_o}{R_L}$$

$$I_{C1} = \frac{V_{CC}}{R_1} - I_{B2} = \frac{V_{CC}}{R_1} - \frac{I_C}{h_{FE2}} - \frac{V_o}{h_{FE2}R_L}$$

I_{C1} must be $\geqslant 0$ even when

$$I_C = I_{C\,max} \simeq \frac{V_{CC}}{R};\ V_o = V_{o\,max} \simeq V_{CC}$$

and

$$h_{FE2} = h_{FE2\,min}$$

We therefore have

$$\frac{V_{CC}}{R_1} - \frac{V_{CC}}{h_{FE2\,min}R} - \frac{V_{CC}}{h_{FE2\,min}R_L} \geqslant 0,$$

from which

$$R_1 \leqslant h_{FE2\,min}\frac{RR_L}{R + R_L} \quad \ldots\ldots\ldots\ (1)$$

The value of R_1 has been chosen according to the above equation, and this resistor must, therefore, be switched together with R.

Equation 12a of the Appendix is a good approximation if $G \gg 1$. Considering also the initial step voltage, we have

$$V_A = \left[\Delta V_o + \frac{V_{CC} - V_T}{RC}t\right]\frac{R_L + R_R}{R_L + R_R + R_6}$$

The threshold voltage of the trigger is given by $V_S = V_D - V_1$, where V_1 takes account of the different voltages dropped across D_4 and D_5 on the one hand, and D_2 and the base-emitter diode of T_3 on the other. V_1 is only slightly affected by the voltage and is equal to 0.5 V.

By taking $V_A = V_S$ the delay time T of the timer can be derived as follows:

$$V_D - V_1 \simeq \Delta V_o + \frac{V_{CC} - V_T}{RC}$$

from which

$$T \simeq RC \frac{V_D - V_1 - \Delta V_o}{V_{CC} - V} \quad \ldots\ldots\ldots\ldots (2)$$

Any inconsistency between the value of delay calculated according to (2) and the measured value is within 2% even for the longest delays.

ERROR ANALYSIS

Errors are due essentially to two causes: variations of the supply voltage from its nominal value (24 V) and temperature variations. Errors resulting from the first condition are very slight indeed. In fact, an examination of Equation (2) shows that both the numerator and the denominator are proportional to V_{CC} of V_1 and the initial step voltage ΔV_o are neglected (ΔV_o contains the component V_{D1} that is not proportional to V_{CC}). Bearing in mind that the terms not proportional to V_{CC} mentioned above are of the order of a few per cent in relation to V_D, it is clear that a constant delay can be obtained over a wide range of variations in supply voltage. Experimental results show that variations in V_{CC} of ±50% of nominal value cause the delay to vary by less than 3%, while the variation of delay time caused by ±20% variations of V_{CC} is quite unnoticeable.

The effects of temperature variations are more conspicuous, however, and can be summarized as follows:

(a) variations of V_{BE} and of transistor gain
(b) leakage currents in T_1 and T_2
(c) presence of leakage currents in D_1 and D_2
(d) variations of the insulation resistance of capacitor C.

As has already been shown, variations of V_{BE} in the integrator have an insignificant effect, and the trigger has been compensated by providing D_4 and D_5.

Variations in h_{FE} do not noticeably affect the linearity of the output voltage (see Appendix) but do cause the bias current of T_1 to change. This current change, through the capacitor, causes the slope of V_o to vary. In order to limit the error, the values chosen for R_1 are very close to the maximum values derived from (1).

By evaluating the ratio

$$\frac{I_{B1}}{I_C},$$

the maximum and average errors ($h_{FE} = h_{FE\,min}$ and $h_{FE} = h_{FE\,typ}$ respectively) due to variations of h_{FE} of ±25% can be calculated. It was observed that the average error is less than ±0.5% over the entire range, while the maximum error is less than ±1% for delays below 100s and varies from ±1% to ±2.5% for delays between 100 and 1000s. It should be remembered that an increase of temperature causes an increase in the delay time.

The figure for I_{CBO} of T_1 given in the data sheet is 5 nA maximum at 50°C; the resulting error can be 2% for a delay of 1000s but, since the error is inversely proprotional to the delay time, it rapidly falls to an insignificant value as the delay decreases. The effect of I_{CBO} tends to assist that caused by variations of h_{FE}.

Because of the low reverse voltage applied across D_1, the maximum leakage current flowing is less than 4 nA at 50°C. This current produces an error of 1.5% for T = 1000s, which is inversely proportional to the delay time but tends to oppose that produced by variations of h_{FE}.

The use of Mylar capacitors will ensure that variations of capacity are less than ±1%, and changes in the value of insulation resistance (9000MΩ at 25°C) cause an error approximately equal to 0.2%.

The error due to variations of resistance can safely be disregarded if resistors having a low coefficient of temperature are used.

In conclusion, the performance of the timer may be summarized as follows:

(a) the average error over the range (1-1000s) is less than 1%.
(b) the maximum error remains at ±2% for delays between 1 and 100s inclusive, and would only rise to between 4% and 5% for the longest delay in the most unlikely event that the h_{FE} of the transistors was equal to the minimum value, and that at the same time the leakage currents were maximum and errors tending to oppose that due to the variations of h_{FE} were totally absent.

ACKNOWLEDGEMENTS

The authors wish to thank Mr. B. Murari for his useful suggestions.

REFERENCE

E. Wolfendale, "The Junction Transistor and its Applications," p. 308, 1958.

APPENDIX

Analysis of a Miller Integrator Using a Current Amplifier.

Referring to Fig. 1(a), G is the current gain of the amplifier and R_i is the input resistance. A capacitor C is connected between the input and output of the amplifier and a step voltage V is instantaneously applied to the input via a resistance R.

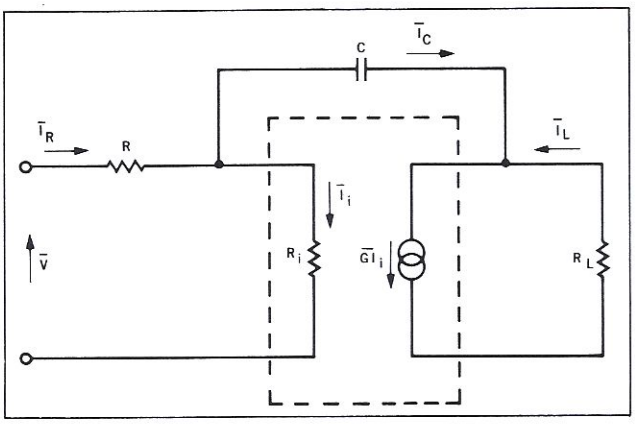

Fig. 1(a). Equivalent circuit of a Miller integrator.

The following equations apply:

$$(R + R_i)\bar{I}_i + R\bar{I}_c = \bar{V}$$

$$G\bar{I}_i - \bar{I}_L - \bar{I}_c = 0 \quad \ldots\ldots (1a)$$

$$R_i\bar{I}_i + R_L\bar{I}_L - \frac{\bar{I}_c}{pC} = 0$$

where $\bar{I}_i$, $\bar{I}_L$, $\bar{I}_c$ are functions of the complex variable p.

Solving in terms of $\bar{I}_L$, we have

$$\bar{I}_L = \bar{V}\frac{G + pCR_i}{R + R_i + pC[RR_L(1 + G) + R_i(R + R_L)]} \quad (2a)$$

Given that

$$R' = \frac{RR_L(1 + G) + R_i(R + R_L)}{R + R_i} \quad \ldots\ldots (3a)$$

we obtain

$$\bar{I}_L = \bar{V}\frac{G + pCR_i}{(R + R_i)(1 + pCR')} \quad \ldots\ldots (4a)$$

Since it is assumed that V is a step function, $\bar{V} = \frac{V}{p}$

and therefore

$$\bar{I}_L = \frac{V}{R + R_i}\left[\frac{G}{p(1 + pCR')} + \frac{CR_i}{1 + pCR'}\right]. \quad (5a)$$

from which

$$\bar{I}_L = \frac{VG}{R + R_i}\left[\frac{1}{p} - \frac{1}{p + \frac{1}{CR'}}\right]$$

$$+ \frac{VR_i}{(R + R_i)R'}\frac{1}{p + \frac{1}{CR'}} \quad \ldots\ldots (6a)$$

Using the inverse Laplace transform, we have

$$I_L = \frac{VG}{R + R_i}\left[1 - \exp(-t/CR')\right]$$

$$+ \frac{VR_i}{(R + R_i)R'}\exp(-t/CR') \quad \ldots\ldots (7a)$$

If $CR' \gg t$, the series development of the exponential produces

$$I_L \simeq \frac{VG}{R + R_i}\cdot\frac{t}{CR'} + \frac{VR_i}{(R + R_i)R'}\left[1 - \frac{t}{CR}\right]. \quad (8a)$$

$$I_L \simeq \frac{Vt}{(R + R_i)CR'}\left[G - \frac{R_i}{R'}\right] + \frac{VR_i}{(R + R_i)R'}. \quad (9a)$$

which is a linear function of time.

If the current gain of the amplifier is sufficiently high, R' can be made much greater than R_i, so that

$$I_L \simeq \frac{VGt}{C[RR_L(1 + G) + R_i(R + R_L)]} \quad \ldots (10a)$$

If the gain G is high and R_i is low, the second term of the denominator can be ignored; the output voltage is therefore given by

$$V_o = -\frac{G}{G + 1}\cdot\frac{Vt}{CR} \quad \ldots\ldots (11a)$$

Since G is much greater than 1, this simplifies to

$$V_o = -\frac{V}{CR}t \quad \ldots\ldots (12a)$$

which is independent of G.